A method of testing an integrated circuit

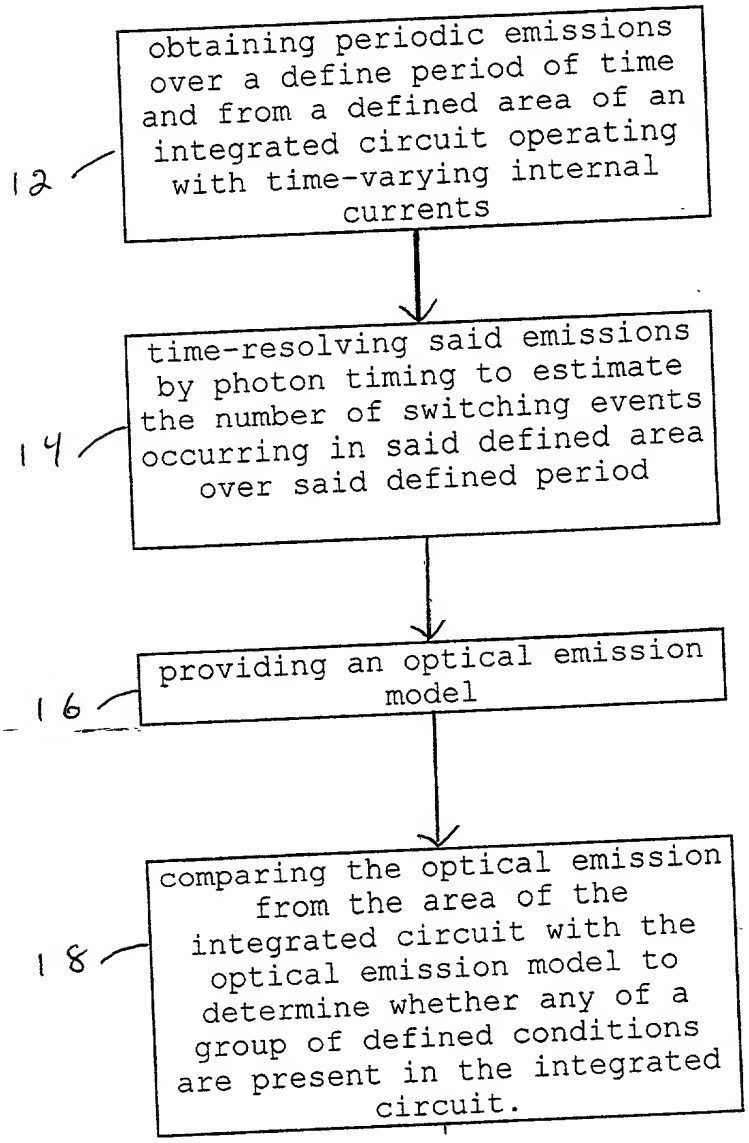

Figure 1

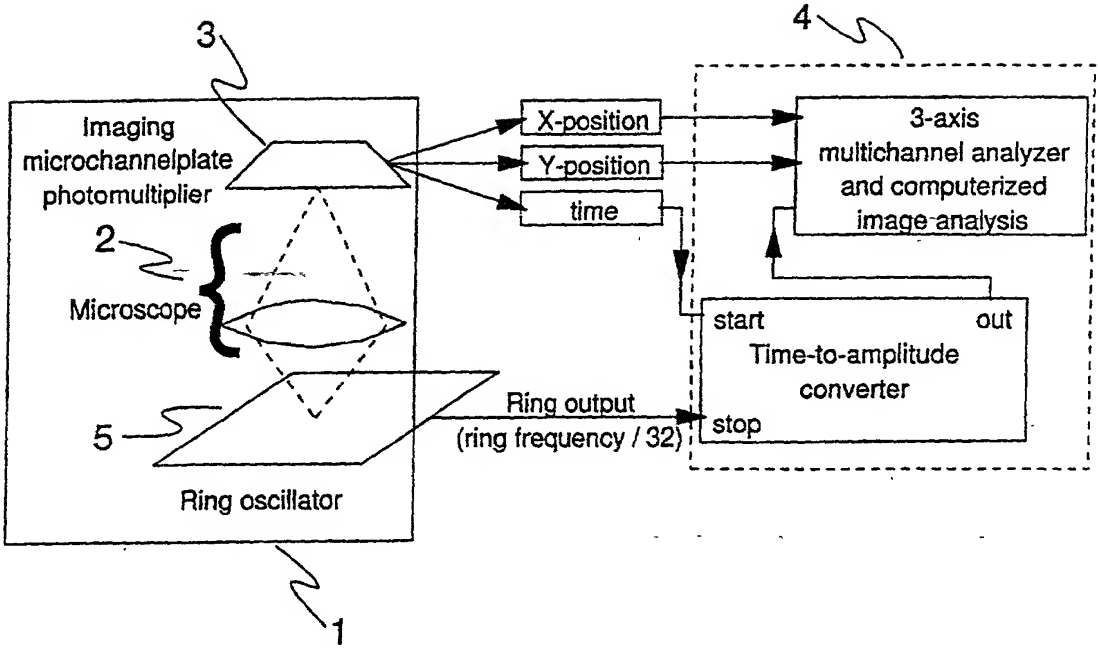

Figure 2